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Notice of Allowability	Application No.	Applicant(s)	
	10/825,647	SLATER ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the filing of the application papers on 15 April 2005*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 7/8/05
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

This office action is in response to the filing of the application papers on 15 April 2004. Claims 1-20 are pending.

Allowable Subject Matter

Claims 1-20 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest a method of fabricating a plurality of light emitting devices where a plurality of spaced apart mesa regions are formed epitaxially on a substrate, the mesa regions including therein a diode region; defining first reduced area regions on the mesa regions; forming a multilayer conductive stack that includes a barrier layer on the first reduced area regions of the mesa regions; forming a passivation layer on the substrate between the mesa regions, on exposed portions of the mesa regions and on exposed portions of the multilayer conductive stacks, the passivation layer defining second reduced area regions on the multilayer conductive stacks; forming a bonding layer on the second reduced area regions of the multilayer conductive stacks; and dicing the substrate between the mesas to produce the plurality of light emitting diodes.

For example, Seabaugh et al. (5,422,305) disclose a method of fabricating a plurality of light emitting devices where a first reduced area regions are defined on a

substrate; and forming a multilayer conductive stack that includes a barrier layer on the first reduced area regions (Fig. 6a-6d; col. 4, line 15 thru col. 5, line 59). However, Seabaugh et al. do not disclose, anticipate, teach, or suggest epitaxially forming a plurality of spaced apart mesa regions on a substrate, the mesa regions including therein a diode region; forming a passivation layer on the substrate between the mesa regions, on exposed portions of the mesa regions and on exposed portions of the multilayer conductive stacks, the passivation layer defining second reduced area regions on the multilayer conductive stacks; forming a bonding layer on the second reduced area regions of the multilayer conductive stacks; and dicing the substrate between the mesas to produce the plurality of light emitting diodes.

Shigeyuki et al. (JP 11-121803) disclose a method of fabricating a plurality of light emitting devices where a plurality of spaced apart mesa regions are formed on a substrate, the mesa regions including therein a diode region; defining first reduced area regions on the mesa regions; forming a conductive stack on the first reduced area regions of the mesa regions (fig. 2; solution). However, Shigeyuki et al. do not disclose, anticipate, teach or suggest epitaxially forming the plurality of spaced apart mesa regions on a substrate; forming a multilayer conductive stack that includes a barrier layer on the first reduced area regions of the mesa regions; forming a passivation layer on the substrate between the mesa regions, on exposed portions of the mesa regions and on exposed portions of the multilayer conductive stacks, the passivation layer defining second reduced area regions on the multilayer conductive stacks; forming a bonding layer on the second reduced area regions of the multilayer conductive stacks;

and dicing the substrate between the mesas to produce the plurality of light emitting diodes.

Kish, Jr. et al. (6,015,719) disclose a method of fabricating a plurality of light emitting devices where a plurality of spaced apart mesa regions are formed epitaxially on a substrate, the mesa regions including therein a diode region; defining first reduced area regions on the mesa regions; forming a multilayer conductive stack that includes a barrier layer on the first reduced area regions of the mesa regions; and dicing the substrate between the mesas to produce the plurality of light emitting diodes (Fig. 7a, 7b & 8; col. 5, lines 8-56). However, Kish, Jr. et al. do not disclose, anticipate, teach or suggest forming a passivation layer on the substrate between the mesa regions, on exposed portions of the mesa regions and on exposed portions of the multilayer conductive stacks, the passivation layer defining second reduced area regions on the multilayer conductive stacks; forming a bonding layer on the second reduced area regions of the multilayer conductive stacks; and dicing the substrate between the mesas to produce the plurality of light emitting diodes.

The prior art made of record in this action does not anticipate, teach, or suggest a method of fabricating a plurality of light emitting devices where a plurality of spaced apart mesa regions are formed epitaxially on a substrate, the mesa regions including therein a diode region; defining first reduced area regions on the mesa regions; forming a multilayer conductive stack that includes a barrier layer on the first reduced area regions of the mesa regions; forming a passivation layer on the substrate between the mesa regions, on exposed portions of the mesa regions and on exposed portions of the

multilayer conductive stacks, the passivation layer defining second reduced area regions on the multilayer conductive stacks; forming a bonding layer on the second reduced area regions of the multilayer conductive stacks; and dicing the substrate between the mesas to produce the plurality of light emitting diodes.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

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